OCR 1.4 Performance

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Revision history

Bernhard Sputh	Creation	02.08.2011
Bernhard Sputh	PPC complete	03.08.2011
Bernhard Sputh	Updated PPC figures	04.08.2011
Bernhard Sputh	Added TI C6000 figures	04.08.2011
Bernhard Sputh	Added ARM-Cortex-M3	11.08.2011
Bernhard Sputh	Added XMOS Figures	15.08.2011

1. Introduction

2. ARM

2.1 Code Size

The given code sizes are measured by compiling different examples with Compile-Option `Os' and Debug-Option `0', see Table 1.

	PI Enabled		PI Disabled	
	Elf .text segment	Mapfile Analysis	Elf .text segment	Mapfile Analysis
Baseline	204	NA	204	NA
Port Only	3412	3176	2800	2564
Full	4236	4000	3620	3384

Table 1: Code sizes for ARM-Cortex-M3

2.2 Semaphore Loop Time

Compile-switch:

- O0: 4555 cycles per loop (.text = 7776 byte)
- O3: 2405 cycles per loop (.text = 4232 byte)
- Os: 2360 cycles per loop (.text = 3640 byte)

2.3 Interrupt Latency

The figures were obtained using the LatencyDemo example shipped with OpenComRTOS-Designer. Thus the code-size includes MP support and a TCP-IP driver.

Compile-switch:

- O0: .text= 32940 byte,
  - IRQ → ISR: 15 – 164 cycles, 50% 20 cycles
  - IRQ → Task: 1100 – 2250 cycles, 50% 1550 cycles
- O3: .text= 23024 byte
  - IRQ → ISR: 15 – 103 cycles, 50% 20 cycles
  - IRQ → Task: 600 – 1200 cycles, 50% 750 cycles
- Os: .text= 18448 byte
  - IRQ → ISR: 15 – 81 cycles, 50% 20 cycles
  - IRQ → Task: 600 – 1200 cycles, 50% 800 cycles

3. PowerPC

3.1 Code Size

The given code sizes are measured by compiling different examples with Compile-Option `Os' and Debug-Option `0', see Table 2.

	PI Enabled		PI Disabled	
	Elf .text segment	Mapfile Analysis	Elf .text segment	Mapfile Analysis
Baseline	1192	NA	1192	NA
Port Only	9724	8300	8700	7128
Full	11260	9764	10236	8584

Table 2: Code sizes for PowerPC e600

3.2 Semaphore Loop Time

Compile-switch:

- O0: 3612 cycles per loop (.text = 30128 byte, includes 12188 byte of Interrupt Vector Table)
- O3: 1638 cycles per loop (.text = 24416 byte, includes 12188 byte of Interrupt Vector Table)
- Os: 1649 cycles per loop (.text = 22388 byte, includes 12188 byte of Interrupt Vector Table)

3.3 Interrupt Latency

The following measurements were generated by using the `sc' instruction, which causes a software interrupt to happen. An external interrupt will have a higher IRQ->ISR latency.

Compile-switch:

- O0: .text= 30128 byte, includes 12188 byte of Interrupt Vector Table
  - IRQ → ISR: 81 cycles
  - IRQ → Task: 1726 cycles
- O3: .text= 24440 byte, includes 12188 byte of Interrupt Vector Table
  - IRQ → ISR: 70 cycles
  - IRQ → Task: 896 cycles
- Os: .text= 22388 byte, includes 12188 byte of Interrupt Vector Table
  - IRQ → ISR: 70 cycles
  - IRQ → Task: 904 cycles

4. TI C6000 Port

4.1 Code Size

The given code sizes are measured by compiling different examples with Compile-Option `Os' and Debug-Option `0'. Table 3 gives the measured code sizes.

	PI Enabled		PI Disabled	
	Elf .text segment	Mapfile Analysis	Elf .text segment	Mapfile Analysis
Baseline	1344	NA	1344	NA
Port Only	9460	6080	8436	5056
Full	11220	7648	10164	6592

Table 3: TI C66x port Code sizes in bytes

4.2 Semaphore Loop Time

Measured with the C6670 cycle approximate simulator from TI and revision 2586 of OpenComRTOS 1.4. Program is running in `L2 SRAM'.

Compile-switch:

- O0: 6283 cycles per loop (.text = 12788 byte)
- O3: 4470 cycles per loop (.text = 11380 byte)
- Os: 5259 cycles per loop (.text = 10068 byte)

4.3 Interrupt Latency

Measured with the C6670 cycle approximate simulator from TI and revision 2586 of OpenComRTOS 1.4. Program is running in `L2 SRAM'.

Compile-switch

- O0: .text = 13076 bytes
  - IRQ → ISR: 131 cycles
  - IRQ → Task: 1764 cycles
- O3: .text = 11508 bytes
  - IRQ → ISR: 136 cycles
  - IRQ → Task: 1367 cycles
- Os: .text = 10196 bytes
  - IRQ → ISR: 136 cycles
  - IRQ → Task: 1572 cycles

5. XMOS

5.1 Code Size

The given code sizes are measured by compiling different examples with Compile-Option `Os' and Debug-Option `0', see Table 4.

	PI Enabled		PI Disabled	
	Elf .text segment	Mapfile Analysis	Elf .text segment	Mapfile Analysis
Baseline	596	NA	596	NA
Port Only	6030	NA	5076	NA
Full	7590	NA	6612	NA

Table 4: Code sizes for XMOS XS1-G4

5.2 Semaphore Loop Time

Measured with the XMOS XC-1 board (XS1-G4) using a single core and revision 2597 of OpenComRTOS 1.4.

Compile-switch:

- O0: 3312 cycles per loop (.text = 8234 byte)
- O3: 2156 cycles per loop (.text = 6310 byte)
- Os: 2130 cycles per loop (.text = 6334 byte)

5.3 Interrupt Latency

The figures were obtained using the LatencyDemo example shipped with OpenComRTOS-Designer. Thus the code-size includes MP support and an UART device and driver.

Compile-switch:

- O0: .text= 14042 byte,
  - IRQ → ISR: 76 – 182 cycles, 50% 77 cycles
  - IRQ → Task: 800 – 1,600 cycles, 50% 1,200 cycles
- O3: .text= 11016 byte
  - IRQ → ISR: 72 – 142 cycles, 50% 73 cycles
  - IRQ → Task: 600 – 1,100 cycles, 50% 800 cycles
- Os: .text= 10740 byte
  - IRQ → ISR: 73 – 139 cycles, 50% 88 cycles
  - IRQ → Task: 600 – 1,100 cycles, 50% 700 cycles